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An Ultralow Power Mixed Dimensional Heterojunction Transistor Based on the Charge Plasma pn Junction

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Development of a reliable doping method for 2D materials is a key issue to adopt the materials in the future microelectronic circuits and to replace the silicon, keeping the Moore's law toward the sub-10 nm channel length. Especially hole doping is highly required, because most of the transition metal dichalcogenides (TMDC) among the 2D materials are electron-doped by sulfur vacancies in their atomic structures. Here, hole doping of a TMDC, tungsten disulfide (WS_2) using the silicon substrate as the dopant medium is demonstrated. An ultralow-power current sourcing transistor or a gated WS_2 pn diode is fabricated based on a charge plasma pn heterojunction formed between the WS_2 thin-film and heavily doped bulk silicon. An ultralow switchable output current down to 0.01 nA μm^{-1}, an off-state current of $\approx 1 \times 10^{-14}$ A μm^{-1}, a static power consumption range of 1 fW μm^{-1}–1 pW μm^{-1}, and an output current ratio of 10^3 at 0.1 V supply voltage are achieved. The charge plasma heterojunction allows a stable (less than 3% variation) output current regardless of the gate voltage once it is turned on.

1. Introduction

Transition metal dichalcogenides (TMDC) are expected to be candidate materials to keep the current trend of miniaturization of microelectronics.[1] To continue the Moore's law below 10 nm channel length and to overcome the short channel effect, the thickness of a channel material also needs to be reduced.[2] TMDC has an advantage over bulk semiconductor materials in terms of switching performance when its thickness approaches atomic thickness.[3] Besides of its atomic thickness, TMDCs have no dangling or broken bonds on their surfaces, which gives another advantage over silicon by suppressing scattering of the charge carriers from the surfaces.

However, TMDCs have major issues hindering its adoption in microelectronics to replace the silicon; one is the reduction of the contact resistance, and the other one is the modulation of doping. Formation of Schottky barrier between a contacting metal and a TMDC is known from the early stage of the TMDC research.[4] Ohmic contacts have been demonstrated by several methods, such as insertion of graphene between the metal and TMDC,[5] or use of a specific metal, like Bi.[6] Thus there has been progress toward realizing the ohmic contact on the TMDC. The most intensively researched TMDC materials, such as MoS_2, WS_2, HfS_2, $HfSe_2$ are electron-doped (n-doped or n-type) materials due to the sulfur vacancies,[7] and $MoSe_2$, $MoTe_2$, WSe_2 are ambivalent.[4] There are lots of on-going efforts to find a stable and reliable hole-doping (p-doped or p-type) method for the above materials,[8] albeit the number of reports on the p-doping is still relatively smaller than that of the n-doping. Representatively, there are three groups of method, charge

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transfer, substitution, and intercalation to achieve the p-doping. Charge transfer doping refers to a doping method in which charge transfer interaction happens between the hosting TMDC and any adjacent dopant medium including molecules,[9] or particles.[10] Because the dopants lie outside of the host material, the charge transfer doping avoids lattice distortion and enables high mobility transport. However, due to the pristine surface of 2D materials, charge transfer doping effects from adsorbates are usually unstable. The second doping method is substitution. Cation elements (metal atoms) can be replaced by elements such as niobium,[11] to achieve p-type doping during its growth. Anion atoms (chalcogen atoms) can be replaced by phosphorus.[12] A patternable doping can be achieved by exposure to the plasma. However, lattice distortion or lattice defects lead to performance degradation. Intercalation method uses the van der Waals nature of the 2D materials. Cu,[13] can be intercalated between layers of SnS_2. The limitation of this technique is the relatively long intercalation time and irrelevance to monolayer materials.

In this article, we report a new charge transfer doping method using a heavily hole-doped silicon substrate as a dopant medium. Based on the method, we could convert a segment of an n-type 2D material into p-type, and fabricated an ultralow power switching device containing a pn junction. Our device can be operated at a 0.1 V supply voltage with 10 pA μm^{-1} output current and 1 pW μm^{-1} static power consumption. The leakage current was reduced down to 0.5 fA μm^{-1}, and the magnitude of the forward current could be controlled by changing the supply voltage from 10^{-11} to 10^{-8} A μm^{-1}. A gate voltage could turn on the forward current of the pn junction, and once the gate voltage passed a threshold voltage, the forward current was stable down to 3% of the current magnitude.

2. Device Fabrication

The charge plasma junction refers to a junction between two materials with significantly different carrier concentrations and work functions (φ) like a metal-semiconductor junction.[14–18] When a metal with a large work function ($\varphi_{Metal} > \chi_{Si} + E_{G,Si}/2$) forms a junction with intrinsic silicon (**Figure 1**a), electrons in the silicon conduction band (CB) diffuse into the metal. The excess holes left in Si, referred to as "charge plasma," raise the silicon band at the junction

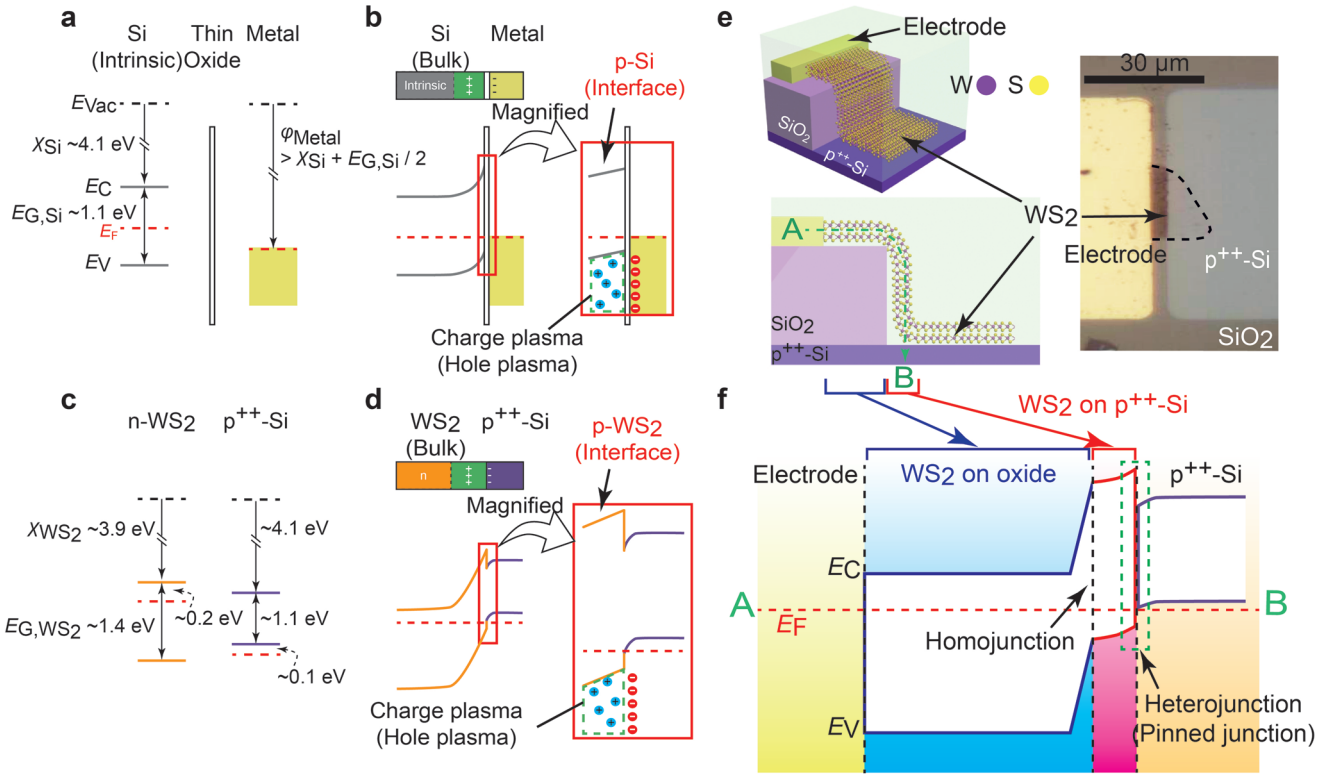

Figure 1. The concept of charge plasma and a device structure with band diagrams. a) Energy bands of intrinsic Si and a metal with large work function before making a junction. The E_{Vac}, χ, E_C, E_G, E_F, and E_V in the figure imply the vacuum level, electron affinity, conduction band minimum, bandgap energy, Fermi level, and valence band maximum, respectively. b) Schematic view of a Schottky junction after making a heterojunction from a). The blue circles describe holes. c) Energy bands of WS_2 and p^{++}-silicon before making a junction. d) Schematic diagram of the Schottky junction after making a heterojunction from c). e) Schematic perspective and cross-sectional view of the device, and an optical image before the gate stack formation. The green dashed arrow between A and B indicates the electron flow path and signifies drawing direction of the band diagram shown in f). f) Band diagram across the carrier flow path between A and B indicated in e). Note that the diagram is not to scale, and its drawing direction does not align just to a single geometrical direction in the real device, but to multiple directions following the current. Note that the band of WS_2 on Si (pink region) follows along the vertical direction inside the WS_2 in the figure e) (see Text S4 and Figure S5 for detailed information, Supporting Information). The pinned junction by the charge plasma is in the green box (see explanation in the main paragraph) and is identical to the magnified view in d).

interface (Figure 1b). If the Si is in bulk form, the energy band rise diminishes gradually away from the interface, recovering its intrinsic nature. If the Si is thin (< 15 nm), the entire Si film remains p-type.[14–16] When a metal with a small work function ($\varphi_{Metal} < \chi_{Si} + E_{G,Si}/2$) forms a junction with Si, the thin Si film becomes n-type.[14–17] Thus, the choice of metal work function determines the doping type of the Si thin-film. There are three conditions responsible for charge plasma,[14–17]: 1) a large difference in mobile charge densities (ratio > 50), 2) a large difference in Fermi levels (> 0.5 eV) in the pairing materials, and 3) a small thickness (< 20 nm) of the less-doped material. The charge plasma phenomenon has been utilized as a technique for doping thin semiconductor film by metals without impurity implantation in simulated or fabricated electronic devices.[14–17] The charge plasma junction is another kind of semiconductor p–n junction, but it is different in several aspects. First, the doping type of the weakly doped semiconductor switches following the heavily doped one. Second, there is no depletion zone at the interface after the junction formation. Finally, doping inversion requires a thin film of the weakly doped semiconductor and a bulk of the heavily doped semiconductor.

Charge plasma was also formed in a pair of thin-film multilayer n-WS_2 and heavily doped bulk Si (p^{++}-Si) as it satisfied the conditions mentioned above in terms of the charge density difference (≈10^{18} cm^{-3} in WS_2,[19] and ≈5×10^{19} cm^{-3} in p^{++}-silicon[20]) and the Fermi level difference (≈1.4 eV). The multilayer WS_2 is known to have an electron affinity, χ_{WS2} of ≈3.9 eV,[21,22] a Fermi level ≈0.2 eV below the CB minimum,[23] and the p^{++}-Si has a Fermi level ≈0.1 eV below the valence band (VB) maximum,[24] (Figure 1c). If the thickness of WS_2 is thin enough (typically less than 20 nm by our choice), then the entire n-WS_2 contacting the p^{++} Si will be converted into p-WS_2 in the same manner as a Si/metal junction (Figure 1d). Figure 1e shows a fabricated device where a thin WS_2 flake (≈5.6 nm, confirmed by atomic force microscopy, AFM) was used. The WS_2 flake was transferred across an edge of a 30 nm thick SiO_2 window on the p^{++}-Si substrate via a dry transfer method (see Text S1 (i.e., Text S1, Supporting Information) and Figure S1 (i.e., Figure S1, Supporting Information) for details about the dry transfer and AFM of the WS_2 flake.), followed by Ni/Au contact electrode deposition (see Text S2 for an explanation for why we ignored the effect of the metal contact on our device characteristics, Supporting Information). The flake lies across an oxide step, having a curvature due to the oxide edge. In this report, we assume that the curvature does not affect the electronic band structure of the WS_2. Figure 1f illustrates the energy band diagram along the current path (the green dashed arrow between A and B in Figure 1e). At the WS_2/Si heterojunction, WS_2 contacting Si converts to p-type due to the charge plasma. On the other hand, the WS_2 located on the oxide keeps its natural n-type doping state. Thus, a p–n homojunction is created inside WS_2 across the oxide window.

3. Results and Discussion

Figure 2a shows the current – supply voltage (I–V_S) characteristics of the device shown in Figure 1e (black curve). In the measurements throughout this article, p^{++}-Si was grounded (GND) and $Vs > 0$ V in the text signifies the forward bias and

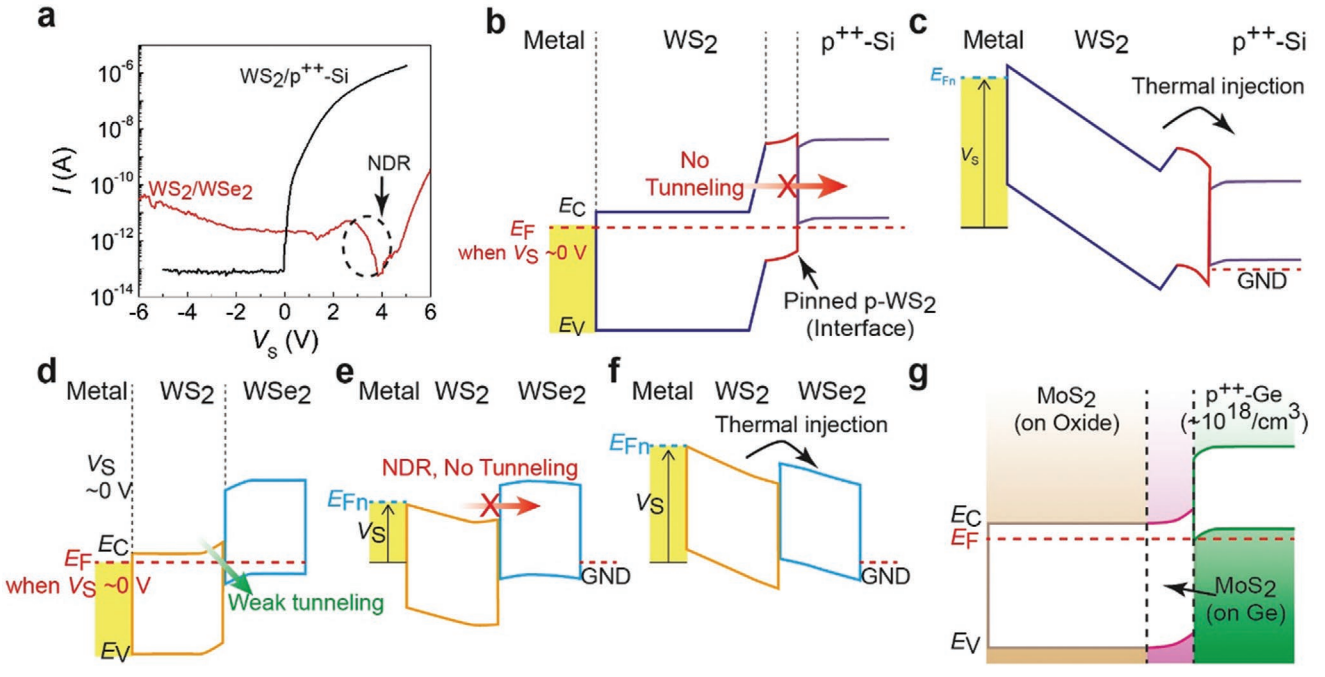

Figure 2. Channel band structure by the charge plasma heterojunction and comparison with a 2D/2D junction. a) Output characteristics under forward bias (Si or WSe_2 is grounded) from the two devices, WS_2/p^{++}Si and WS_2/WSe_2 junction devices. b) A band diagram of the WS_2/p^{++}-Si when V_S close to 0 V, and c) when $V_S > 0$ V. d–f) Schematic band diagrams of WS_2/WSe_2 heterojunction under increasing V_S explaining the NDR. For above diagrams, the electron doping density of WS_2 is assumed to be 10^{18} cm^{-3}, the hole doping density of p^{++} Si to be 5×10^{19} cm^{-3}, and the hole doping density of WSe2 to be 10^{18} cm^{-3}.

$V_S < 0$ V is the reverse bias (i.e., the opposite polarity to the actually applied bias to the metal contacting WS_2), while V_S in the graphs implies the amplitude of the potential energy. The gate potential, V_G has the same polarity with the actually applied bias both in the text and in the graphs. A monotonous increase in I was observed with increasing Vs because the p-WS_2 energy band at the heterojunction was pinned at the Si energy band regardless of V_S (i.e., the energy band alignment modulation dependence on V_S is negligible). The strength of the dipole electric field across the interface due to the charge plasma would be much higher than the local electric field applied at the junction by the metal contact. The pinned p-WS_2 acts as a barrier limiting the thermal or tunneling current (Figure 2b). When Vs > 0 (Figure 2c), the electrons flow over the WS_2 homojunction and WS_2/Si heterojunction entering the CB of p-WS_2 by thermal injection. This thermal process explains the monotonous increasing current observed in Figure 2a. The pinned junction is unique in the WS_2/p^{++}-Si ($\approx 5 \times 10^{19}$ cm^{-3}) charge plasma junction because pinning was not observed in a less hole-doped Si ($\approx 10^{18}$ cm^{-3}),[25] junction. We claim that these two phenomena (i.e., the doping inversion of a TMDC by the charge plasma and observation of the pinned junction effect by a highly asymmetrically doped p–n semiconductors junction) are reported experimentally for the first time.

The characteristics of the black curve in Figure 2a are different from the p–n heterojunction between TMDCs, where the negative differential resistance (NDR),[26,27] or NDR-like,[28,29] features were observed. The NDR feature arises during the transition of transport phenomena between the tunneling and the thermal injection across the junction, depending on the supply bias. To make an experimental comparison, we prepared an n-type WS_2/p-type WSe_2 ($\approx 10^{18}$ cm^{-3}),[30] junction device, replacing the p^{++}-Si with a WSe_2 thin flake (Text S3, Supporting Information). The red curve in Figure 2a acquired from the device clearly shows the NDR, demonstrating the unpinned p–n junction described in Figure 2d–f. The unpinned junction originates from the lack of the charge plasma by the lightly doped WSe_2 and the small difference in Fermi levels ($\approx$0.15 eV).[31] Comparing the curves in Figure 2a, we concluded that the absence of NDR and the pinning of the WS_2/p^{++}-Si junction originated from the charge plasma.

To confirm the observation, we simulated and verified the appearance of the charge plasma and the p–n homojunction in WS_2 across the p^{++}-Si/SiO_2 edge (see Text S4 for details on the simulation tool, material properties used in the simulation, and the simulation results, Supporting Information). In the simulation, Si doping concentration strongly correlates to the WS_2 doping inversion (see Figure S6 for the effects from doping concentration difference and from material difference, Supporting Information). Due to the doping inversion, a built-in potential (φ_{bi}) of $\approx$1.07 eV is generated across the homojunction (Figure 2b). The n-WS_2/p-WS_2 homojunction forms a step-shaped energy bandstructure along the conduction path inside the WS_2, and the stepping homojunction effectively amplifies the WS_2 bandgap to $\approx$2.5 eV from its intrinsic bandgap ($\approx$1.4 eV),[21] emulating a larger bandgap material.

Figure 3a shows a schematic of the same device with a gate stack. Using a gate configuration, WS_2 channel under the gate could be divided into two separate regions: a region on the oxide (region I), and a region on the p^{++}-Si (region II). Figure 3b shows the output characteristics of the device under gate voltage (V_G) sweep, and Figure 3c,d displays the energy band diagrams depending on the relative magnitude of V_G. We characterized the switching operation of the device with V_S from 0.1 to 4.6 V and V_G sweep from −5 to 5 V (for the full data up to V_S = 7.1 V with hysteresis, see Text S5, Supporting Information). The cause of the hysteresis is the gate oxide because if the channel was covered by hexagonal boron nitride (hBN) as a gate oxide the hysteresis was removed (see Figure S14 for hBN effect, Supporting Information). The leakage current through the gate dielectric Al_2O_3 was measured simultaneously and its magnitude was kept at the noise level (Figure S7b, Supporting Information), confirming the switching operation was by the V_G. The switching mechanism can be explained by the gate field effect on regions I and II. For example, when the V_S was 1.6 V and the V_G was −2 V, the device was off. In this configuration, the charge carrier flow is blocked by the bandgaps of region I and II (Figure 3c and location A in Figure 3b). When V_G was −1 V, the device started to turn on. When V_G was increased to 1 V, the device was fully on (Figure 3d and location B in Figure 3b) with a subthreshold swing of 150 mV per decade. Both CB minima of regions I and II are below the quasi Fermi level due to the gate field effect, so the charge carriers reach the CB of Si by overcoming the heterojunction. Once the energy bands of regions I and II are below the quasi Fermi level, V_G does not affect the thermal injection across the pn homojunction anymore. This explains the abrupt saturation and the definite plateauing of the on-current, suggesting a possible application as a current regulator. Figure 3e shows variations of the on-currents of Figure 3b for Vs = 0.1 and 4.6 V only on a linear scale. For the on-currents, the variation (standard deviation divided by an average value of the on-currents of the device in percent) is mostly less than 3% (6% at vs = 0.1 V) (Figure 3f). This value is comparable to a 7% variation of output current reported in a gated-Schottky barrier transistor, which also shows plateauing output current less than a microampere.[32] Although it is not possible to directly compare our device with other sub-microampere current reference circuits, several articles report 8–26% variation of output current due to combined effects from variations in temperature, fabrication process, and supply voltage.[33] Thus, further research is required considering those parameters for a fair comparison of the stability of the output current. The variation of the output current at Vs = 0.1 V in Figure 3e can be understood as the thermal energy of the electrons. Multiplication of the magnitude of the current variation with the output resistance of the device gives the energy of 0.03 eV, which is similar to the thermal energy of electrons at room temperature.

The variation of the on-current in Figure 3b with respect to V_S could be understood as charge transport across the heterojunction. The WS_2/p^{++}-Si junction, while being a junction of semiconductors only, could be approximated as a metal-semiconductor Schottky barrier[34] (**Figure 4**a, inset). To account for the on current dependence on the V_S in the transconductance measurement, the current passing the pn homojunction and the Schottky heterojunction thermally and arriving at the CB of Si, could be described by a following equation[35]

$$I(V_G, V_S) = I_0\left(e^{V_G^s/(sV_T)} - 1\right)e^{-\Phi_B/V_T}\left(e^{(E_{Fn}-E_{F,Si})/V_T} - 1\right) \quad (1)$$

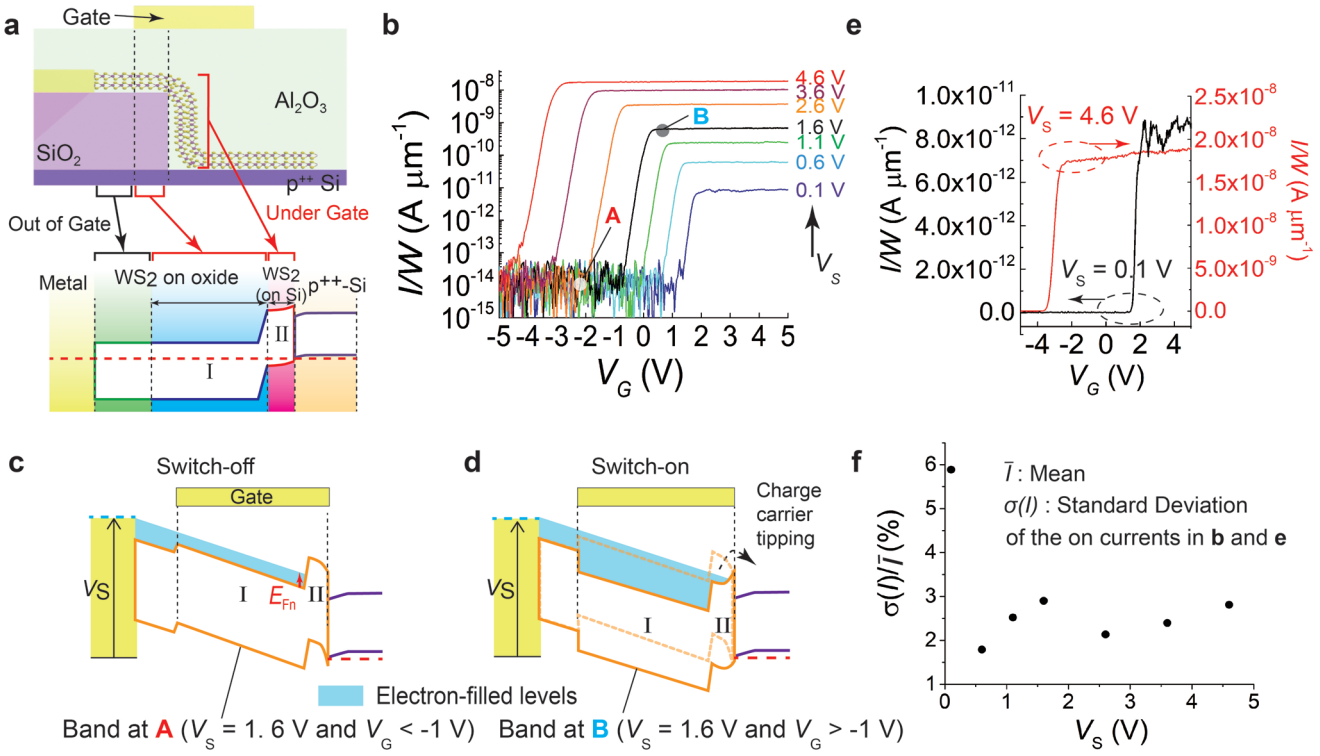

Figure 3. Switching operation for stable output currents. a) Cross-sectional view of the complete device including the gate stack and its band diagram in equilibrium. The band is identical with Figure 1f, but with gate coverage and region designations. b) Output characteristics under forward biases. The best subthreshold swing is 150 mV per decade. The "*W*" in the *y*-axis implies the width of the WS_2 flake, 15 μm. c,d) Bands explaining the switching operation of the device depending on the gate bias. Depending on the magnitude of the V_G, the bandgaps in regions I and II move up or down to allow or to prohibit current flow across the heterojunction. The dashed band in d) indicates the location of the band in c). The red arrow in c) indicates the quasi-Fermi level, E_{Fn}, of region I in WS_2. e) Output current plots from the same datasets of b) in a linear scale for V_S = 0.1 V (black) and V_S = 4.6 V (red). f) On-current deviations ($\sigma(I)/\bar{I}$) for various V_S values from 0.1 to 4.6 V.

where I_0 is the off-current, V_G^* is the gate voltage increase required to raise the current from noise to the saturation level, *s* is a gate field reduction factor (see Text S6 for an explanation of V_G^* and *s*, Supporting Information), V_T is the thermal voltage, Φ_B is the Schottky barrier height, and E_{Fn} is the quasi-Fermi level in the region II against the Fermi level in the silicon. Equation (1) is the multiplication of the Shockley diode equation and the Schottky diode equation, where V_S-*IR* in the original Shockley diode equation is replace by V_G*, because in the transconductance measurement, V_S is fixed and V_G has the role of V_S in a diode. The Φ_B and E_{Fn} are functions of V_S, but they are not functions of V_G. When V_S rise, both Φ_B and E_{Fn} will rise accordingly. Because we did not know their exact numerical relationships, we assumed that Φ_B did not vary significantly compared to E_{Fn}. Thus, we could calculate the shift of E_{Fn} against the Fermi level of Si, $E_{F,Si}$, at the saturated current. Figure 4a shows the calculated $E_{Fn} - E_{F,Si}$ (blue triangles) for various V_S. Using this information, we could calculate Φ_B. The red squares in the same figure confirm that Φ_B does not vary significantly compared to E_{Fn}. From the variations of E_{Fn} and Φ_B under V_S, we can understand the characteristics of the on-current in Figure 3b. Namely, the rise of E_{Fn} allows more electrons to overcome the Schottky barrier, but the increase in E_{Fn} is less significant at higher V_S. The gate threshold voltage $V_{g,th}$ depends on V_S (Figure 3b). This dependency can be explained as the variation of quasi-Fermi level, E_{Fn} in the region I due to V_S. When V_S increases, for example, from 1.6 to 2.6 V, E_{Fn} in region I (red arrow in Figure 3c) will rise. Then, the $V_{g,th}$ required for electrons to overcome the homojunction barrier decreases, shifting from −0.9 to −2 V. The $V_{g,th}$ dependency on V_S results in various controllable transfer characteristics and on-current modulation.

To verify the energy band model in Figure 3 from a different perspective, we swept the V_S under various V_G. Figure 4b shows the output characteristics of the device under negative V_G, and Figure 4c–e display the energy bands depending on the magnitude of V_S. When $V_S \leq 0$ and $V_G = -3$ V (location C in Figure 4b), there was no current flow since the flow of charge carriers is blocked by the energy bandgaps of regions I and II in the WS_2 (Figure 4c). When a small positive V_S (< 1 V) was applied under $V_G = -3$ V, such as at location D in Figure 4b, the current flow was still not observed (Figure 4d). At the V_S, the E_{Fn} in region I is not high enough to overcome the homojunction barrier. However, when $V_S > 1$ V applied (location E in Figure 4b), the device was on. The raised V_S can increase the E_{Fn} and carrier concentration in region I, and the height of the homojunction barrier is reduced, so that carriers can be injected into CB of region II and Si (Figure 4e). The supply voltage threshold $V_{s,th}$ depends on V_G. For example, when V_G was −5 V, the energy bands I and II would be raised beyond

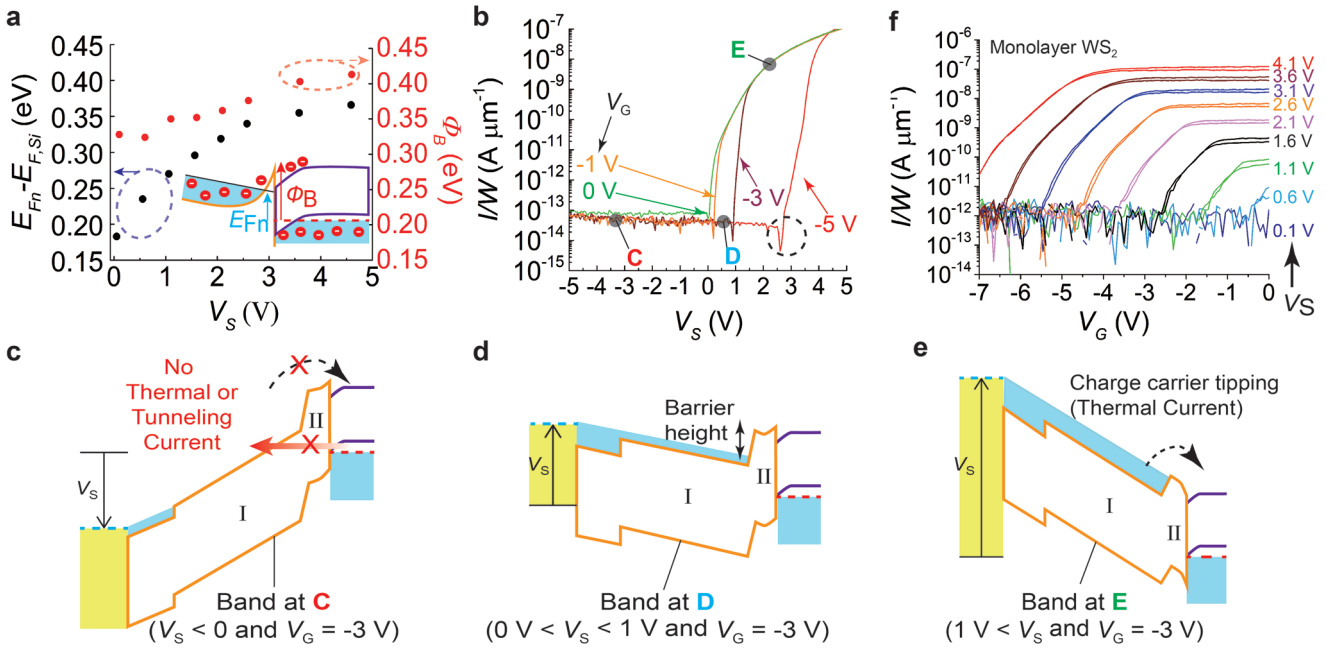

Figure 4. Proof of band structure by V_s–I scans and a monolayer device. a) Variation of the quasi-Fermi level, E_{Fn}, and Schottky barrier height, Φ_B, depending on the supply bias. Inset: Schematic diagram explaining the Schottky junction at the hetero interface. b) Supply voltage sweep results with various gate biases. c) Band diagram explaining the off-state observed in b when $V_S < 0$. d) Band diagram when $0\ V < V_S < 1\ V$ and $V_G = -3$ V. e) Band diagram explaining on-state when $1\ V < V_S$ and $V_G = -3$ V. f) Gate sweep results from an identical device based-on a monolayer WS_2 (refer to Text S12 for details, Supporting Information). The best subthreshold swing is 300 mV dec^{-1}.

their levels at $V_G = -3$ V. Then, the relatively smaller E_{Fn} in region I can make the charge carrier transport over the homojunction more difficult, thus requiring a larger $V_{s,th}$ like ≈2.5 V. In contrast, if V_G were –1 or 0 V, lowered regions I and II could make the carrier transport easier, thus requiring a smaller $V_{s,th.}$

Our device has a pn homojunction and a Schottky junction simultaneously along the channel. Thus the diode mechanism of the on current as observed in Figure 4b needs to be identified for clear understanding. Either of the diffusion model across the pn junction or the thermionic emission across the Schottky junction can explain the on current in Figure 4b. To clarify this issue, we did low temperature measurements (**Figure 5**a,b). If thermionic emission model is right, the off-state current is $I_0 = AA^{**}T^2\exp(-q\phi/kT)$, where A is the diode area, A^{**} is the Richardson constant, T is the absolute temperature, q is the unit charge, φ is the Schottky barrier height, and k is the Boltzmann constant. When the Richardson plot is plotted, where $\mathrm{Ln}(I_0/T^2AA^{**})$ lies along vertical axis, and $1/T$ in horizontal axis, the barrier height can be obtained by fitting the data points with a strait negative slope as $-q\phi/k$. In Figure 5a, there are two I–V_S graphs when $V_G = 0$ V at 77 and 300 K. Because the off current of 77 K measurement was too small to be detected by our measurement (below the minimum detectable current level, a few 10^{-13} A μm^{-1}), we cannot make the Richardson's plot. Instead, we can use measurements when $V_G = 2$ V in Figure 5b. If the magnitudes of the two off currents at $V_s = -8$ V in the 77 and 300 K graphs are inserted in the off-current equation, the value, $\mathrm{Ln}(I_0/T^2AA^{**})$ gives –14.5 at 1/77 K^{-1}, and –18 at 1/300 K^{-1}, resulting in a positive slope. That is a negative barrier height and this calculation results rejects the thermionic explanation on the observations in Figure 5a,b. Thus, the diffusion correctly explains the exponential current increase of the plots. According to the diffusion theory,[36] the current follows the Shockley equation, $I = I_0(\exp(qV/kT) - 1)$. But the low temperature graph in Figure 5a suggests that there is an additional term, $\varphi_{bi} \approx 1$ eV such that $I = I_0(\exp(q(V_S - \phi_{bi})/kT) - 1)$. We believe that this φ_{bi} is the activation energy, because the quasi-Fermi level in the region I needs to raise above the built-in potential across the pn homojunction, depicted as the double headed black arrow in Figure 4d, to turn on the current. Also this value agrees our simulation result on the pn homojunction barrier height (≈1.07 eV). Additionally, the barrier height can be measured in another method, capacitance–voltage (CV) measurement. If a CV measurement under a reverse bias is plotted as $1/C^2$ versus V_S, the x-intercept gives the value. Figure 5c shows the measurement, and the x-intercept was ≈1.5 eV, which was larger than the expected value of φ_{bi} ≈1 eV. We interpret that this value can be the sum of the φ_{bi} across the pn homojunction and the Schottky barrier height (≈0. 35 eV) at the heterojunction. The small remaining deviation (≈0.15 eV) might came from additional parasitic capacitances in the device (such as capacitance between the gate electrode and the channel). In conclusion on the diode mechanism, the diffusion process across the pn junction correctly describes the I–V_S relationships in our device.

We characterized the static power consumption of the device. According to the results shown in Figure 3b, when V_S is 1.1 V, the static or off-state power consumption is about 10^{-14} W μm^{-1}. These values are comparable to the static power consumption of an oxide semiconductor device operating in the deep subthreshold regime.[37] Furthermore, when V_S was reduced to 0.1 V, the power consumption was further decreased to about

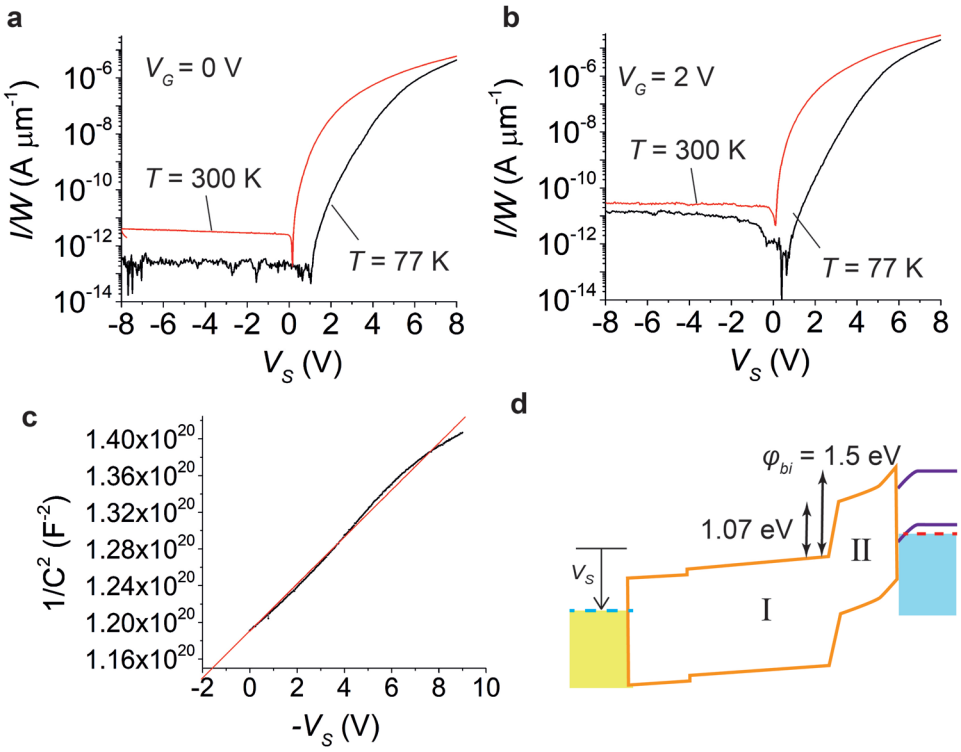

Figure 5. Proof of thermal switching mechanism by low temperature measurements and *C–V* measurement. a, Supply voltage sweep when $V_G = 0$ V at two different temperatures, 77 and 300 K. b) Supply voltage sweep when $V_G = 2$ V at the same temperatures. c) Capacitance–voltage measurement of the device, when a reverse bias ($V_S < 0$) was applied to the metal contact and $V_G = 0$ V. f) Interpretation of the measurement in c) as the summation of the barriers of pn homojunction and the Schottky junction.

10^{-15} W μm^{-1}. These ultralow quiescent power characteristics likely result from the effectively amplified (≈2.5 eV) WS_2 bandgap. When the device is off, the charge carriers are not blocked just by the nominal WS_2 bandgap but by an effectively amplified bandgap (≈2.5 eV) that is much larger than 1.4 eV. Compared to the conventional substrate-gated field-effect transistors (FETs) based on a WS_2 thin-film, the off-currents of the device are at least 10 times smaller (Figure S9, Supporting Information), even though the measurement of the off-currents is limited due to our measurement limit (10^{-13}–10^{-14} A μm^{-1}). This novel ultralow current switching mechanism using the pseudoamplified energy band structure as a switch, may provide an alternate way to demonstrate ultralow-power current sourcing transistors.

We explored the device as an amplifier (Text S7, Supporting Information). In the investigation, we obtained an intrinsic gain and cut-off frequency of 70 V V^{-1} and 170 kHz at $V_S = 7.1$ V. The parameters indicate that our device is better than Si metal-oxide-semiconductor field effect transistor(MOSFET) in terms of intrinsic gain. For assessing our device as a diode, we used the Shockley diode equation to extract the diode ideality factor, *n*, and we obtained a minimum of 1.5, which suggests a similar rectification performance (mostly in the range of 1–2) compared to other mechanically exfoliated TMDC materials based diodes (Text S8, Supporting Information).[38–44] The small current dips (dashed circle) before turning on the current at $V_G = -5$, −3, and −1 V in Figure 4b may have originated from the potential well existing at the heterojunction (Text S9, Supporting Information).

The measurements from a chemical vapor deposition (CVD)-grown monolayer WS_2/p^{++}-Si device shown in Figure 4f suggest an identical switching mechanism (Text S10, Supporting Information). However, the device exhibits normally-on characteristics with a lower on-off current ratio than multilayer WS_2/p^{++}-Si. We attribute the normally-on characteristic to the smaller pn homojunction barrier height inside the monolayer WS_2. A smaller homojunction barrier means weaker charge plasma, and weaker charge plasma may originate from a smaller Fermi level difference between the monolayer WS_2 and Si. The location of the Fermi level in a CVD-grown few-layer WS_2 was reported at 0.8 eV,[45] below the CB minimum, which implies less n-doping in the CVD-grown WS_2 than the exfoliated one. Therefore, a CVD-grown monolayer WS_2 results in a smaller $V_{g,th}$. The lower on-off current ratio cannot be explained solely by monolayer thickness because the difference in the on-current at the same V_S is larger than the thickness ratio between the monolayer and multilayer flake (≈0.7–0.8 vs ≈5.6 nm). A possible explanation is based again on the smaller n-doping state of the CVD-grown monolayer WS_2. In that case, the rise of E_{Fn} with increasing V_S is significantly smaller than the multilayer WS_2, resulting in a much smaller on-current. The subthreshold swing of the device is much larger (300 mV per decade) than the one based on the exfoliated material (150 mV per decade). This can be explained by a much larger number of charge traps existing at the surfaces of the material, because the CVD-grown film has a relatively larger number of defect sites than exfoliated ones and the defect sites act as charge traps.[46] Thus, the electrostatic field

by the traps will screen the field from the gate potential. Finally, the energy band structure and the operation principle were verified from other devices including another WS_2 devices with difference thickness (8.5 and 2.6 nm) and MoS_2 or SnS_2-based devices (Text S11, Supporting Information). From this consideration, we can conclude that the operation principle of the WS_2, MoS_2, and SnS_2-based devices are analogous to the WS_2-based device in Figure 1.

4. Conclusion

In conclusion, a novel way to hole dope a 2D material and to generate an ultralow-power steady current-sourcing transistor has been proposed and verified. The performance has been achieved through the charge plasma pn heterojunction, which simply made out of a contact between the TMDC material and silicon. As a result, an ultralow stable current of 0.01 nA μm^{-1} with a supply voltage 0.1 V was achieved, enabling ultralow-power reference current applications. The new p-doping method reported in this article is the first experimental demonstration on the doping conversion into p-type of sub-10 nm TMDC material by electrostatic doping,[47] and will be useful for development of diverse novel electronic devices based on TMDC materials-based pn or bipolar junctions.

5. Experimental Section

Device Fabrication and Electrical Measurement: A 525 µm thick heavily p-type (100)-oriented Si (0.001 Ω cm, boron doping concentration of $\approx 10^{20}$ cm^{-3}) with dry oxidation of 30 nm thick silicon dioxide wafer was used to make the charge plasma heterojunction. We exposed the silicon surface by dry etching of the oxide layer using CF_4:O_2 = 6:1 mixing gas with an RF power of 30 W at 5 mTorr. A 70×70 μm^2 area of the oxide was etched, and a flake of WS_2 was transferred across the edge of the silicon window through the dry transfer method (Text S1, Supporting Information). For electrical contact to the silicon, a corner of the wafer was scratched to expose the silicon surface, and a probe tip was contacted at the corner. Both the deposited metal electrode and the wafer corner served either as a source or a drain depending on the polarity of the potential. All the junction areas, including the electrode, were covered by a 30 nm thick Al_2O_3 grown by atomic layer deposition at 100 °C. A gate electrode was formed covering the flake across the oxide edge using thermal evaporation of 10/70 nm thick Ni/Au. Finally, a 180×180 μm^2 area of Al_2O_3 was etched to make electrical contact with the metal electrode in contact with WS_2. After device fabrication was complete, a B1500a semiconductor device analyzer (Keysight) was used to obtain output curves and transfer curves at room temperature in a dark-box probe station.

Monolayer WS_2 Film Growth and Device Fabrication: The sample consisted of a tungsten source carrier chip (5 nm WO_3 on 90 nm SiO_2 on Si) and bare SiO_2/Si substrate (90 nm thick SiO_2, WRS materials). Tungsten oxide (WO_3, 99.99%, Kurt J. Lesker) was utilized as the tungsten source, deposited on SiO_2 via electron beam evaporation. The tungsten source chip was covered, in face-to-face contact, by a bare SiO_2/Si substrate as the growth substrate. The sample was loaded into the center of a 3 in diameter and 1 m long quartz tube (MTI Corp.), and a ceramic boat with 0.8 g of sulfur powder (99.98%, Sigma-Aldrich) was located upstream in the quartz tube. The location of the ceramic boat containing the sulfur powder was calculated so that the sulfur melted at 780 °C. The furnace was an MTI 1200×1-zone furnace. After loading, the ambient gas of the tube was purged out via a mechanical pump to the base pressure of 400 mTorr. The furnace was heated to 700 °C at a 20 °C min^{-1} ramping rate and then to 900 °C at 5 °C min^{-1}. 60 sccm of Ar gas (5.0 UH purity, Praxair) was introduced at 150 °C (increasing temperature) to reduce moisture inside of the tube and was discontinued at 600 °C (decreasing temperature). Hydrogen (40 sccm, 5.0 UH purity, Praxair) gas was supplied to improve WO_3 reduction from 700 °C (increasing temperature) to 600 °C (decreasing temperature). The growth pressure was 7 Torr. After 25 min at 900 °C, the furnace was cooled down to room temperature.

Statistical Analysis: For the calculation of the values, $\sigma(I)$ and $\overline{I}$ in the graph of Figure 3f, following methods are used. 1) Preprocessing of data—the current values in Figure 3e were divided by the width of the WS_2 flake to normalize the output current value per channel width. 2) Data presentation—$\sigma(I)$ is the standard deviation of the normalized output current, I, and $\overline{I}$ is the mean value of the output current. 3) Sample size (n) of each statistical values—For the calculations of $\sigma(I)$ and $\overline{I}$, 82 data from V_S = 0.1 V graph and 203 data from V_S = 4.6 V graph were used. Only the turned-on output currents were used in those graphs. 4) Statistical methods used to assess significant differences with sufficient details—$\sigma(I)$ and $\overline{I}$ are simply for reporting of the values, not for accessing of a hypothesis or a theoretical claim. 5) Software used for statistical analysis—OriginPro 2016.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

diodes, doping, heterojunctions, homojunctions, silicon, transistors, transition metal dichalcogenides

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