A Nanochannel Fabrication Technique without Nanolithography

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ABSTRACT

We have developed a new nanochannel fabrication technique using chemical-mechanical polishing (CMP) and thermal oxidation. With this technique, it is possible to control the width, length, and depth of the nanochannels without the need for nanolithography. The use of sacrificial SiO₂ layers allows the fabrication of centimeter-long nanochannels. In addition, the fabrication process is CMOS compatible. We have successfully fabricated an array of extremely long and narrow nanochannels (i.e., 10 mm long, 25 nm wide, and 100 nm deep) with smooth inner surfaces.

Introduction. Nanofabrication of extremely small fluidic structures provides powerful tools for the field of bionanotechnology.¹⁻⁴ Nanochannels are essential components in nanofluidic systems. Among the many requirements for the nanochannel fabrication technique are the following: It should be cost-effective, able to precisely control channel dimensions, and be CMOS compatible for ultimate integration with microelectronics. Previously, various nanochannel fabrication techniques based either on e-beam lithography, step sidewalls, or laser machining have been reported.⁵⁻⁷ However, these techniques suffer from several limitations. For example, e-beam lithography-based processes are relatively expensive.⁵ The step sidewall approach has limitations in the maximum possible lengths of the nanochannel because of lateral sacrificial etching effects.⁶ Finally, laser machining can only produce nanochannels with minimum widths in the range of a few hundred nanometers and the fabrication process is not CMOS compatible.⁷ In this paper, we describe the demonstration of a cost-effective nanochannel fabrication technique with precisely controlled dimensions, using a conventional CMOS fabrication process.

Experimental Section. Figure 1 shows the fabrication procedures. First, 100 nm thick amorphous silicon is deposited as shown in Figure 1a. The deposited amorphous silicon thickness determines the depth of the nanochannel. The photolithography is performed for determining the length and shape of the nanochannel. And it is etched using reactive ion etch (RIE) and subsequently oxidized in 1000 °C dry O_2 for 40 min, as shown in Figure 1b. The SiO₂ thickness is about 50 nm, which determines the width of the nanochannel. Thus, the width of the nanochannel is controlled by adjusting SiO₂ film thickness with the oxidation temperature or time.⁸ The lower limit of the width in the nanochannel is about 5



Figure 1. Fabrication procedures. (a) SiN_x and first amorphous Si deposition; (b) RIE and dry O_2 oxidation for the nanometer gap; (c) second amorphous Si deposition; (d) CMP until the gap oxide is exposed. (e) The oxide in the nanometer gap is etched. (f) The Au or oxide layer is used for sealing.

nm, because the dry O_2 oxidation can readily produce 5 nm SiO₂ film. And 500 nm thick amorphous silicon is deposited as shown in Figure 1c. The overlayer thickness is approximately five times that of the amorphous silicon layer, to minimize "dishing" effects. CMP process is performed to expose the gap oxide as shown in Figure 1d. Then, the gap oxide is vertically etched in the (10:1) buffered oxide etch (BOE) for 20 min as shown in Figure 1e. The oxide in

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Figure 2. SEM micrographs of nanochannel array with Au sealing at different magnification: (a) low and (b) high magnification. The width is about 50 nm.

the nanometer gap is fully etched in just 20 min, because the gap oxide is etched before sealing the nanochannel. In addition, there is no limitation in the length of the nanochannel, because the sealing process is performed after etching the sacrificial oxide.^{6,8} Finally, evaporated gold or PECVD SiO₂ is used to seal the nanochannels as shown in Figure 1f. SiO₂ sealing is very attractive for biomedical applications due to transparent optical properties for fluorescence detection. The fabricated nanochannel has a very smooth inner surface due to the property of the amorphous silicon. However, it has the hydrophobic surface property, which is not good for the liquid flowing along the nanochannel. Before the nanochannel is sealed, a thermal oxidation process can be performed for changing the surface property from hydrophobic to hydrophilic. In addition, the width of less than 5 nm can be obtained, because the channel becomes narrower due to the growth of the oxide in the sidewall during this oxidation. We can also make the fluidic channel, with width in the nanometer to micrometer range, by using silicon nitride as oxidation a masking layer. Then, we can easily access the nanochannel through the microchannel.

Results and Discussions. Figure 2 shows the fabrication results of the nanochannel with Au sealing. Figure 2a shows the nanochannel array with low magnification. Figure 2b shows high magnification of the nanochannel of which the width, depth, and length are 50 nm, 100 nm, 10 mm, respectively. Figure 3 shows the nanochannel in high magnification with PECVD SiO_2 sealing. The width is



Figure 3. SEM micrograph of nanochannel with PECVD oxide sealing: The width is approximately 25 nm.

approximately 25 nm, which is reduced from 50 nm gap distance due to the deposition of the oxide in the sidewall during PECVD process. Thus, the surface property of the nanochannel is hydrophilic due the hydrophilic property of the oxide.

Conclusions. We demonstrated a cost-effective CMOS compatible nanochannel fabrication technique using CMP and thermal oxidation processes without nanolithography. We also successfully fabricated a nanochannel with the width of 25 nm. The width, depth, and length can be precisely controlled by thermal oxidation, deposited film thickness, and photolithography, respectively. The sacrificial SiO₂ is etched before the nanochannel is sealed, allowing the sacrificial oxide to be easily removed. The reported nanochannel fabrication technique can be applied in the detection of individual DNA sequences or proteins by a passing single molecule through the nanochannel.

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References

- Foquet, M.; Korlach, J.; Zipfel, W.; Webb, W. W.; Craighead, H. G. Anal. Chem. 2002, 74, 1415.
- (2) Burns, M. A., et al. Science 1998, 282, 484.
- (3) Turner, S. W.; Perez, A. M.; Lopez, A.; Craighead, H. G. J. Vac. Sci. Technol. B 1998, 16(6), 3835.
- (4) Desai, T. A.; Chu, W. H.; Tu, J. K.; Beattie, G. M.; Hayek, A.; Ferrari, M. Biotechnol. Bioeng. 1998, 57(1), 118.
- (5) Matsumoto, K.; Kawakami, T.; Nakao, M.; Hatamura, Y.; Kitamori, T.; Sawada, T. Proc. IEEE MEMS 1998, 127.
- (6) Tas, N. R.; Berenschot, J. W.; Mela, P.; Jansen, H. V.; Elwenspoek, M.; van den Berg, A. *Nano Lett.* **2002**, 2(9), 1031.
- (7) Hui, A. P.; Qin, S.-j.; Li, W. J.; Wang, M. Y. Proc. IEEE MEMS 2002.
- (8) Lee, C.; Lee, J.; Han, C. IEEE Electron Device Lett. 2000, 21 (10), 479.
- (9) Cao, H.; Yu, Z.; Wang, J.; Tegenfeldt, J. O.; Austin, R. H.; Chen, E.; Wu, W.; Chou, S. Y. Appl. Phys. Lett. 2002, 81 (1), 174.

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